are no longer held in abeyance in this application as noted in the response filed on June 22, 2001. However, when the non-elected claims were canceled in the paper filed May 1, 2001, a typographical error was followed in which claims 13 to 27, rather than claims 23 to 27 and claims 28 to 51 were canceled as directed to groups II and III. Therefore, please reinstate claims 13 to 22, all of which are in the elected group I, are depending directly or indirectly on claim 1, and read on the elected species of Figs. 3, 9 and 13, if claim 1 is generic.

New claims 52 and 53 are added, in which claim 52 reads only on Fig. 4 and would be allowable if claim 1 is allowable, while claim 53 reads on Fig. 3.

As to this application, prosecution continued with the election of Group II, having claims 1 to 22, drawn to a semiconductor device.

Subsequent to that election, however, an election of species requirement was made as to claims 1 to 12. The Examiner contended that there were five patentably distinct species, i.e. embodiment 1 of Figures 3, 9 and 13; embodiment 2 of Figs. 4 and 15; embodiment 3 of Fig. 14; embodiment 4 of Fig. 16, and embodiment 5 of Figures 17 and 18. A response to this requirement provisionally elected the species of embodiment 1, drawn to Figures 3, 9 and 13, on which claims 1, 2, 6 and 9 were alleged to be generic to all of the species, while at least claims 4, 7, 10 to 12, and at least 14 to 17 were alleged to read on the elected species of embodiment 1, Figs. 3, 9 and 13.

This response was not disputed by the Examiner as to this election, wherein claims 3, 5 and 8, all remaining claims of this elected Group not alleged to read on embodiment 1, were withdrawn from consideration. These claims are eligible for reinstatement if claims generic to all of the species, or generic to a subgroup of species including those claims are allowable. The error in inadvertently canceling originally elected claims 13 to 22 is regretted.

This procedural history is stated because of the increasing procedural complexity of this prosecution. The objections and rejections are thus now responded to. It is again noted that a preliminary amendment making changes to the specification and certain of the claims under scrutiny was filed on May 02, 2000; thus, it is that version of the claims and specification that is under consideration.

Objection to Claim 9

Claim 9 had been objected to for improving its clarity, without making a rejection to that effect. According, the correction required by the Examiner has been made in this response, with appreciation to the Examiner for a thorough review and helpful suggestion for clarification.

Rejection of Claim 4

Claim 4 had been rejected for its use of a "PN type electroconductivity". This should have referred to an FN electroconductivity referring to a Fowler-Nordheim (FN)

conductivity, consistent to claims 1 and 2, for example. Withdrawal of this rejection is appropriate.

Rejection of Claims 1, 2, 6, 7 and 9 to 12

These claims were initially rejected as allegedly being anticipated by the patent to Yamauchi, No. 5,877,054. This initial rejection is respectfully traversed.

The initial rejection as phrased fails to make a prima facie case of anticipation in that the Yamauchi reference seems not to include a gate insulating film that includes a FN type tunneling film which has an FN type tunneling characteristic. It seems that the Examiner in his discussion of Fig. 1 does not allege otherwise, but rather refers generally to Figs. 1 to 51.

In explaining the rejection, it is requested that the Examiner "compare at least one of the rejected claims feature by feature with the prior art relied on in the rejection" MPEP, section 1208. While the examiner started to do this, he failed to "align the language of the claim side-by-side with a reference to the specific page, line number, drawing reference number, and quotation from the prior art, as appropriate". Ibid. Furthermore, the Applicant must be apprised of where the claimed features are found in the reference and are alleged to meet the limitations of the claims.

The claims as originally presented may well have been confusing to the Examiner, and have now been amended to clarify the structure and to overcome the section 112 rejection, a

discussion of which follows, before reverting again to a discussion of the nature of the Applicant's invention.

Rejection of Claims 1, 2, 6, 7 and 9 to 12 under 35 USC 112

This rejection is well-taken for claim 1 may appear to have a double inclusion of the elements. Accordingly, claim 1 is amended to recite the main features of the inventive gate insulating film 6 of Fig. 3, including the tunneling film that reads at least on layer 10 with or without the nitride film 12. Support for the revisions to claim 1, and the addition of new claims 52 to 53 are found in the specification as filed, especially at pages 18 to 43. There, it will be indicated how the newly-added claims read on the elected Fig. 3 and, where appropriate, are generic to each of the species that formed the basis for the election of species requirement for the elected invention.

Response to the Anticipation and Obviousness Rejections

A first step in handling a claim involves giving its terms appropriate meaning. Claim 1 uses "means plus function" language for its recitation of the charge storing means provided in the tunnel insulating film and in the gate insulating film," said to be facing to the surface of the channel forming region in the substrate. See page 22 for a definition of "channel forming region", the paragraph spanning pages 23 and 24 for a discussion of the charge forming characteristics of the tunnel insulating

film 10, and pages 24 to 31 for discussions seriatim for such charge storing means in the gate insulating film and in the tunnel insulating film and their interrelationship, as well as their relationship between the gate insulating film and the substrate. It is not seen that Yamauchi, because of its floating gate structure, meets this limitation when properly interpreted in accordance with precedent governing 35 USC 112, sixth paragraph. See the applicable sections of the MPEP.

But, in any case, Yamauchi does not appear to anticipate or render obvious the Applicant's claimed invention, without further specificity as to the points allegedly found in the reference. In contrast, Yamauchi relates to a nonvolatile semiconductor memory using a FN tunnel current for writing and erasing. Col. 1, lines 11 to 17. However, insofar as understood, the technology of Yamauchi relates to memories involving floating gates, see generally col. 1, lines 27 to 49, col. 7, lines 54 to 64. Note also the summary discussion indicating a relationship between the floating gate and the source or drain diffusion regions, see col. 7, line 65 to col. 8, line 52.

Claim 1 thus is amended to distinguish the Applicant's invention from that of Yamauchi, as understood. It is submitted that one of ordinary skill in the art would not be placed in possession of the invention of the Applicant, as claimed, because of the flash memory/floating gate disclosure of Yamauchi. In the

absence of "mapping" at least a representative claim on Yamauchi, it is not seen where in Yamauchi the Examiner is finding the limitations of the original claims.

The rejection of claim 4 is traversed. In that rejection, the Examiner alleges that all of the claimed limitations are met, except for the FN films there stated. There is no teaching or suggestion of forming the gate insulating film of the Applicant with a nitride film, for example, or teachings of suitable nitride films.

As originally presented, the claim 1 as amended recites a gate insulating film 6 (see Figs. 3 and 4) formed "on" the semiconductor channel forming region 1a and comprising an FN type tunneling film which has an FN type tunneling electroconductivity and contains material having a dielectric constant greater than that of the silicon oxide. As to this latter limitation, the Examiner only cited "Figures 1 to 51 of Yamauchi" to support that finding. Greater specificity is solicited to properly respond. Reexamination and reconsideration is respectfully requested.

Respectfully submitted,

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APPENDIX
AMENDED CLAIMS

1. (Amended) A nonvolatile semiconductor memory device comprising a plurality of memory elements formed in the vicinity of the surface of a substrate, a plurality of word lines for driving the memory elements, and a plurality of bit lines,

each of said plurality of memory elements including:

a semiconductor channel forming region formed in the vicinity of the surface of the substrate,

a source region in contact with the channel forming region in the vicinity of the surface of the substrate,

a drain region in contact with the channel forming region at a position facing the source region in the vicinity of the surface of the substrate,

a gate insulating film, including a tunnel insulating film, formed on said substrate adjacent to the channel forming region,

a top insulating film formed on said gate insulating film;

a conductive gate electrode formed on the top insulating film on the gate insulating film, and

a charge storing means facing said surface of the channel forming region and which is provided in the tunnel insulating film and in the gate insulating film and is planarly dispersed to the other neighbor charge storing means in the gate insulating film;

[a] the gate electrode of the plurality of memory elements being respectively connected to the plurality of word lines;

wherein said [a] gate insulating film formed [on] adjacent to the semiconductor channel forming region [and comprising] comprises a Fowler-Nordheim (FN) type tunneling film which has a FN type tunneling electroconductivity and contains material having a dielectric constant greater than that of silicon oxide;

[a gate electrode formed on the gate insulating film; and

a charge storing means, formed in the gate insulating film, and facing to the surface of the channel forming region].

2. (amended) A nonvolatile semiconductor memory device according to claim 1, wherein the FN type tunneling film comprises any one of a nitride film, an oxynitride film, and aluminum oxide film, a tantalum pentaoxide film and a BST ($BaSrTiO_3$) film, having an FN tunneling electroconductivity.

3. (amended) A nonvolatile semiconductor memory device according to claim 1, wherein the gate insulating film includes a buffer layer formed between the FN type tunneling film and the channel forming region and suppressing an interface trap level.

4. (twice-amended) A nonvolatile semiconductor memory

device according to claim 1, wherein the gate insulating film comprises a Pool-Frenkel (PF) type film including any one of a nitride film, an oxynitridge film, and aluminum oxide film, a tantalum pentaoxide film and a BST ($BaSrTiO_3$) film, having a [PN] FN type electroconductivity.

5. (amended) A nonvoltatile semiconductor memory device according to claim 4, wherein the gate insulating film includes a buffer layer formed between the FN type tunneling film and the PN film.

6. A nonvolatile semiconductor memory device according to claim 1, further comprising:

a pull-up electrode in the vicinity of the gate electrode or a wiring layer connected to the gate electrode, via a dielectric film; and

a pull-up gate bias means for applying a voltage to the pull-up electrode.

7. (previously amended) A nonvolatile semiconductor memory device according to claim 6, wherein

a plurality of gate electrodes of the plurality of memory transistors are connected to a plurality of word lines, and

a selected transistor is connected between the pull-up gate bias means and the pull-up electrode, said pull-up gate bias

means supplying a voltage having a polarity the same as a polarity of a boosting voltage for boosting the precharged word line by a capacitance coupling.

8. A nonvolatile semiconductor memory device according to claim 6, wherein the pull-up electrode is arranged in the vicinity of an upper portion of the gate electrode or a connection layer connected to the gate electrode, via the dielectric film.

9. (twice-amended) A nonvolatile semiconductor memory device according to claim 1, wherein each memory transistor comprises a source region [contracted] contacted to the channel forming region, and a drain region spaced to the source region and contacted to the channel forming region,

wherein a plurality of gate electrodes of the plurality of memory transistors are connected to a plurality of word lines,

wherein the source region and drain region of each memory transistor are connected to a common line in a bit direction, electrically insulated to and intersecting the word line, and

wherein said nonvolatile semiconductor memory device further comprises

a write inhibit voltage supply means for supplying a reverse-biased voltage to the source region and/or the drain region of the memory transistor the gate electrode of which is

connected to the word line selected at a writing, through the common line, to make the source region and/or the drain region in a reverse-biased state to the channel forming region, and

a non-selected word line biasing means for supplying a voltage to a non-selected word line at the writing, a polarity of the voltage being a polarity making the non-selected word line in a reverse biased state to the channel forming region.

10. (previously amended) A nonvolatile semiconductor memory device according to claim 9, wherein the write inhibit voltage supply means supplies the reverse bias voltage to the source region and/or the drain region to make a bias voltage of the memory transistor connected to the selected word line to thereby prevent an erroneous write and/or an erroneous erase.

11. (previously amended) A nonvolatile semiconductor memory device according to claim 9, wherein the non-selected word line biasing means supplies a voltage having a polarity for reverse-biasing to the non-selected word line to make a bias voltage or the memory transistor connected to the non-selected word line to thereby prevent an erroneous write and/or an erroneous erase.

12. (previously amended) A nonvolatile semiconductor memory device according to claim 9, wherein the non-selected word line biasing means biases the gate electrode to the source region

so that a voltage of the gate electrode becomes a low level equal or lower than an inhibit gate voltage.

Please add the following new claims:

Please reinstate the original claims 13 to 22.

52. (newly-added) A non volatile memory device according to claim 1 wherein said gate insulating film includes a buffer layer adjacent said tunnel insulating film and said surface of the substrate.

53. (newly-added) A nonvolatile semiconductor memory device according to claim 1 wherein said gate insulating film includes a tunnel insulating film, a nitride film, and said top insulating film in that order sandwiched between said surface of said substrate and said gate electrode, a portion of said gate insulating film overlapping each of said source region and said drain region.